In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 5 and 15 without prejudice.

1. (Previously Presented) A processing element comprising:

an instruction buffer;

a first most often (MO) buffer coupled to the instruction buffer;

an execution unit coupled to the instruction buffer to execute instructions stored within the first MO buffer based upon a first predetermined profile; ~~and~~

a decode module, coupled to the instruction buffer, the first MO buffer, and the execution unit, to decode an instruction to determine whether the instruction is to be stored in the first MO buffer;

a second MO buffer coupled to the instruction buffer and the decode module;

first profile buffer coupled to the first MO buffer to store the first predetermined profile; and

a second profile buffer coupled to the second MO buffer to store the second predetermined profile.

2. (Currently Amended) The processing element of claim 1 ~~further comprising a second MO buffer coupled to the instruction buffer and the decode module,~~ wherein the execution unit executes instructions stored within the second MO buffer based upon a second predetermined profile.

3. (Cancelled)

4. (Previously Presented) The processing element of claim 2 wherein the decode module decodes an instruction to determine whether the instruction is to be stored in the first MO buffer or the second MO buffer.

5. (Cancelled)

6. (Currently Amended) The processing element of claim 2 ~~5~~ wherein the first and second predetermined profiles each include a plurality of profile bits, each profile bit indicating whether a corresponding instruction is to be executed at the execution unit during a particular instruction fetch cycle.

7. (Original) The processing element of claim 6 further comprising:

a first profile pointer coupled to the first profile buffer; and

a second profile pointer coupled to the second profile buffer.

8. (Original) The processing element of claim 7 wherein the first profile pointer points to a first profile bit of the first predetermined profile during a first instruction fetch cycle.

9. (Original) The processing element of claim 8 wherein an instruction stored in the first MO buffer is executed at the execution unit during the first instruction fetch cycle if the first profile bit is active.

10. (Original) The processing element of claim 8 wherein an instruction stored in the instruction buffer is executed at the execution unit during the first instruction fetch cycle if the first profile bit is inactive.

11. (Currently Amended) A digital signal processor (DSP) comprising:

a plurality of processing elements, wherein each of the processing elements comprises:

an instruction buffer;

a first most often (MO) buffer coupled to the instruction buffer;

a second most often (MO) buffer coupled to the instruction buffer;

an execution unit coupled to the instruction buffer to execute instructions stored within the first MO buffer based upon a first predetermined profile and to execute instructions stored within the second MO buffer based upon a second predetermined profile; ~~and~~

a decode module, coupled to the instruction buffer, the first MO buffer, the second MO buffer and the execution unit, to decode an instruction to determine whether the instruction is to be stored in the first MO buffer or the second MO buffer; and

a first profile buffer coupled to the first MO buffer to store the first predetermined profile; and

a second profile buffer coupled to the second MO buffer to store the second predetermined profile.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Previously Presented) The DSP of claim 11 wherein the first and second predetermined profiles each include a plurality of profile bits, each profile bit indicating whether a corresponding instruction is to be executed at the execution unit during a particular instruction fetch cycle.

17. (Original) The DSP of claim 16 wherein each processing element further comprises:

a first profile pointer coupled to the first profile buffer; and

a second profile pointer coupled to the second profile buffer.

18. (Original) The DSP of claim 17 wherein the first profile pointer points to a first profile bit of the first predetermined profile during a first instruction fetch cycle.

19. (Previously Presented) A method comprising:

receiving a first instruction from an instruction buffer;

examining a bit within the first instruction to determine if the first instruction is to be stored in a first buffer;

determining whether the first instruction includes a command to load a profile if the first instruction has not been designated to be stored in the first buffer; and

loading the profile in a second buffer if the first instruction has not been designated to be stored in the first buffer.

20. (Previously Presented) The method of claim 19 further comprising executing the first instruction.

21. (Previously Presented) The method of claim 19 further comprising:

storing the first instruction in the first buffer if it is determined that the first instruction is to be stored in the first buffer; and

executing the first instruction from the instruction buffer.

22. (Previously Presented) The method of claim 19 further comprising:

retrieving the first instruction from the first buffer if the bit indicates that the first instruction is to be retrieved from the first buffer; and

executing the first instruction after it has been retrieved from the first buffer.

23. (Previously Presented) The method of claim 22 further comprising executing the first instruction after it has been retrieved from the second buffer if it is determined that the first instruction does not include a command to load a profile and if the first instruction has not been designated to be stored in the first buffer.

24. (Previously Presented) An article of manufacture including one or more computer readable media that embody a program of instructions, wherein the program of instructions, when executed by a processing unit, causes the processing unit to:

receive a first instruction from an instruction buffer;

examine a bit within the first instruction to determine if the first instruction is to be stored in a first buffer;

determine whether the first instruction includes a command to load a profile if the first instruction has not been designated to be stored in the first buffer; and

load the profile in a second buffer if the first instruction has not been designated to be stored in the first buffer.

25. (Previously Presented) The article of claim 24 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to execute the first instruction.

26. (Currently Amended) The article of claim 24 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to:

store the first instruction in the first buffer if it is determined that the first instruction is to be stored in the first buffer; and

execute the first instruction from the instruction buffer.

27. (Previously Presented) The article of claim 24 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to:

retrieve the first instruction from the first buffer if the bit indicates that the first instruction is to be retrieved from the first buffer; and

execute the first instruction after it has been retrieved from the first buffer.

28. (Previously Presented) The article of claim 27 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to execute the first instruction after it has been retrieved from the second buffer if it is determined that the first instruction does not include a command to load a profile and if the first instruction has not been designated to be stored in the first buffer.